A 16 channel VLSI chip, containing charge amplifier and analog to digital converter, for readout of highly granular particle detectors


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Abstract

An integrated circuit for readout of particle detectors, producing a charge signal has been developed. The circuit contains 16 channels of charge integration, sample and hold amplifier, followed by an analog multiplexer. The charge content of each channel is digitized, one by one, by a 6 bit nonlinear flash ADC. The result is stored in a memory, pending for readout. The chip has proven to sense an input charge as low as 1 fC. Two versions of the chip exist, one with a gated charge integrator input and the other with a shaping amplifier input stage. Both circuits have been fabricated on large scale. They have successfully been used for readout of multistep avalanche chambers and streamer tube detectors in the Heavy Ion experiment WA98 at the CERN SPS. © 1998 Elsevier Science B.V. All rights reserved.

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1. Introduction

Experiments with Pb beams at ultrarelativistic energies provide extraordinary technical challenges due to the very large number of secondary particles in each reaction. More than a thousand charged particles are emitted in central Pb + Pb collisions at the CERN SPS. In particular, particle tracking is very difficult and projected coordinate measurements must be complemented by space point measurements. The large multiplicity also means that the granularity in the readout system has to be...
larger, by orders of magnitude, compared to what is available with standard techniques.

The Application Specific Integrated Circuit (ASIC) described in this paper has been designed for readout of Multistep Avalanche Chambers (MSAC) [1–5]. This type of detector has a continuous position response in two dimensions (contrary to multiwire proportional chambers). Fig. 1 illustrates the principle of the MSAC with amplification in two steps. The gated function allows operation of the chamber at high gain. Typically, a minimum ionizing particle passing through the chamber results in a cloud of more than 10^7 electrons at the rear end of the chamber where readout sensor pads (at ground potential) are placed. The drift of the electrons through the chamber gas, delays the arrival of the cloud by 1.4 μs compared to the passage of the particle. This inherent delay of the analog information allows the particular design of the preamplifier stage which has a gated input. This gate provides a very sharp time definition of the collected charge.

In this readout system, the negative charge in the cloud, which has a typical diameter of 5 mm (expanded due to diffusion of the electrons in the gas), is collected on a few anode pads (see Fig. 1). The

Fig. 1. The principles of the function of a multistep avalanche chamber. High voltage is applied on the steel meshes producing alternating strong and weak electric fields in which the electrons drift towards the pad plane. The two strong fields (gaps A1, A2) provide amplification in two steps by avalanche multiplication in the chamber gas. By a HV-gate pulse, which switches the field direction in gap G, only triggered events are allowed to develop full gain by two-step amplification. The lower part of the figure illustrates the pad pattern on which the electron cloud, due to the staggered arrangement, spreads out over several pads both horizontally and vertically.
integrated charge on each pad is digitized and in the offline analysis, the centroid of the cloud is calculated. Due to the staggered pad geometry, the cloud spreads over a few pads also in the vertical direction, thus allowing the centroid to be calculated also in this direction.

A tracking system with two planes of these chambers, equipped with ca. 70 000 channels of readout electronics has been built and was successfully used in the WA98 experiment at CERN in 1996. This paper describes the readout chip itself as it is of general interest and it can be used in a variety of applications. It is called the MSAC chip [6] throughout this paper.

A modified version (the STD chip) [6], with the input stage being a shaping amplifier, designed for prompt, positive input charge, has also been produced. It is primarily aimed for pad readout of the Streamer Tube Detectors (STD) in WA98. The two circuits are identical except for the amplifier stage. When this chip is specially referred to we name it the STD chip. This version of the chip has been used in the same experiment to read out approximately 50 000 pads, distributed over an area of 19 m² of streamer tube detectors. The block diagram of the STD chip resembles the one shown in Fig. 2, except for the absence of the trigger level input (trig-lev) and multiplicity trigger output (I trig). Instead, this chip has a control of the shaping time by an external DC-voltage (see below).

The performance of the MSAC and streamer tube detectors, operated with the corresponding ASICs and readout systems will be described in detail in forthcoming papers.

2. Functional description

The new ASIC aims, in particular, at fixed target experiments in which one receives an event trigger.

![Diagram of the MSAC chip and the STD chip](image-url)
and no new event will be taken before the present event has been fully processed. This is an important simplification, because it allows the digital functions to be in standby mode while the preamplifiers are integrating charge. Therefore, it was possible to include both the highly sensitive analog preamplifier and the digital functions in the chip, without much concern about clocknoise and pickup from the digital activity.

Since all chips digitize in parallel, the AD conversion time was not the limiting factor in the envisaged readout architecture. Data readout was designed to be as serial as the detector geometry allowed. Consequently, it was designed for high transfer rates up to 20 MHz.

The block diagram in Fig. 2 shows the principal function of the MSAC chip. All open ended lines in the diagram correspond to an external connection, either a signal in/out or a control voltage. The external connections can also be identified in Fig. 3 which shows a photograph of the chip, bonded to the thin printed circuit board before the circuit was sealed with an epoxy globtop.

2.1. The AD conversion cycle

The amplifier stage operates like a sample and hold circuit which means that the integrated charge is converted to a voltage level which is proportional to the detected charge. This level is kept until the chip is reset.

The voltages, held in each channel is digitized one by one. Digitization of an individual channel, starts by the multiplexer connecting the analog voltage of one channel to the second amplifier stage (factor 4 gain) whose output is analyzed by the AD

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Fig. 3. The silicon chip, bonded onto the printed circuit board. The chip size is $3.6 \times 4.2 \text{mm}^2$. 
converter, made of 64 comparators. The voltage level found by the comparators is encoded to a six bit result which is stored together with a parity bit in the FIFO memory. The whole sequence takes one clockcycle. In order to maintain resolution this clock cycle should not be shorter than 2 μs, mainly governed by the time needed for the analog levels to settle. Fig. 4 illustrates the timing sequence of an event.

2.2. Readout through the FIFO memory

After 16 clockcycles, the AD-conversion of all 16 channels is completed. The FIFO switches to shift mode and the clockfrequency is changed to 20 MHz for readout. The FIFO memory has seven input connections (di 0...di 6) and seven output pins (du 0...du 6). This allows many chips to be connected to each other in a serial chain to readout a large number of chips on the same common bus. All the FIFO memories in one readout chain act like one long FIFO in this phase of the readout.

In the readout architecture a Digital Signal Processor (DSP) receives the data from the first chip in the chain. The DSP performs zero suppression and attaches an address to each ADC value. After a full-event cycle has been completed, the DSP board generates a reset which restores all analog levels and alerts the chip to be ready to accept the next event.

3. The charge amplifier stage

3.1. The MSAC chip

Each of the 16 inputs (in 0...in 15) is connected to a charge integrator which integrates the charge appearing inside the externally supplied gate (gate). The charge is converted to a voltage level which is held until a reset occurs. This function is often called sample and hold. The charge amplifier has a conversion gain of 1 mV/fC and it is designed for low-input capacitance. The noise of the preamp at 10 pF is 0.5 fC according to simulations.

Fig. 4. Timing diagrams for the processing of an event. The total number of clockcycles needed to empty the FIFO is decided by the number of chips connected together multiplied by 16. In this example, channels in 2, in 5 and in 9 have detected nonzero charge.
measurements have verified a noise smaller than 1 fC which was the finest AD-converter resolution used.

3.2. The STD chip

This version of the chip was designed for readout of larocci-type streamer tube detectors [7]. Each pad covers an area of several cm² which amounts to a capacitance at the amplifier input of approximately 20 pF. Contrary to the MSAC chambers, the streamer tubes produce an almost instantaneous positive charge signal on the pad, when a particle passes through the chamber. Therefore, the gated integrator design of the MSAC chip could not be used in this more general kind of application. Typically, in case of the WA98 trigger conditions, a trigger or gate signal can only be supplied to the detector after a delay of about 300 ns, i.e. at a time when the pad signal has disappeared already.

The input circuit was thus modified such that the collected charge in the charge amplifier is discharged with a time constant of typically 1 μs. The actual output of the charge amplifier shaper is then sampled in the sample and hold circuit, at the time of the chip trigger which is derived from the experimental trigger. The timing of the chip trigger is chosen to match the peak of the shaped pulse. All voltages are frozen until being reset as for the MSAC chip. The shaping time can be varied between approximately 0.5 and 2 μs by an externally supplied DC-level.

4. The AD converter

With only six bits available for the digitization of the analog voltage one has to optimize the ADC scale between the resolution and the dynamic range of the measurement. The conversion technique used here is the flash ADC principle with 64 comparators. This provides high flexibility, since the reference levels of the comparators (i.e. the ADC channel numbers) can be chosen according to the needs of the particular application.

The optimal solution, for the rather general request, in order to cover a large dynamic range is to choose the reference levels according to a quadratic scale: \( V = AC^2 \) where \( C \) stands for the ADC channel number and the \( V \) is the voltage to be measured. \( A \) is a calibration factor.

Such a simple approach, however, causes the sensitivity of a channel to depend on the actual DC-level (zero level, pedestal) of the channel. We define the sensitivity as the smallest additional input charge which causes the AD-converter to change its result by one unit from the zero value. Any DC-offset of the signal, e.g. due to external pickup, would influence the sensitivity due to the shift of the quadratic conversion scale, directly affecting the detection efficiency. In order to overcome this problem, the 16 lowest ADC channels satisfy a linear conversion scale, while the remaining 48 channels follow the quadratic scale. The transfer characteristic of the AD-conversion scale is shown in Fig. 5.

The reference levels needed to produce this binning by the comparators are produced by a resistor chain from which the 64 reference voltages are tapped. The ends of this voltage divider are fixed by two externally supplied voltages, ref low and ref high. By adjustment of these two, one can compensate for the DC-offset (average for the channels in the chip) that may be present. The offset would otherwise reduce the useful range of the AD-converter. Likewise, one can make sure that all pedestal values are inside the linear range of the ADC by tuning these control voltages.

Normally, the difference between ref low and ref high is about 3.3 V which corresponds to the largest output amplitude of the \( \times 4 \) amplifier. In this setting one unit of the ADC scale at the sensitive (linear) end, corresponds to 25 mV which means about 6 fC input charge. By reducing ref high, to become closer to ref low one can increase the sensitivity (at the expense of dynamic range) to match the requirements of the application.

5. Additional comments

The MSAC chip is also equipped with a trigger output circuit which sources a 100 μA current on the L_trig output pin if a channel has been hit in the chip. The threshold, over which a channel is
regarded as hit is controlled by an externally applied voltage. Several I−trig outputs can be connected to the same line and the total current pulse is proportional to the multiplicity of hits.

The multiplexed analog signal can be inspected (both chip versions) on the mux output pin where the analog voltage levels are clocked out one after the other.

The power consumption of the chip is very low. The analog part consumes constantly about 10 mW while the digital part takes significant power only during conversion and readout. The average power consumption at typical trigger rates of a few hundred per second is about 1.5 mW per channel.

5.1. Production and large-scale experience

Both chip designs are made for the 1.2 micron channel length CMOS process with double poly capacitors and double-metal interconnects at AMS, Austria. The size of the naked silicon chip (Fig. 3) is 3.6 × 4.2 mm².

The chips, both the MSAC chip and the STD chip have been produced on its own mask set in quantities of ca 5000 each. The chip yield was about 85%. In the yield figure only those chips with fatal errors have been filtered out. No selection was done based on quantitative studies of channel to channel differences, etc. The MSAC chip was used
unpackaged, bonded directly to thin printed circuit boards with the Chip On Board technique. The STD chip was used, packaged in a 44 pin, plastic Quad Flat Package (QFP).

Once a tested chip has been operated for some hours we have not noticed any significant failure rate. In particular, the MSAC chip has been operated in a demanding environment, with occasional high-energy sparks in the multistep avalanche chambers. The charge inputs have standard analog input protection (800 V human body model). No noticable failure rate has been observed during six weeks of continuous, in beam operation.

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References

[6] Detailed questions about the MSAC chip should be directed to A. Oskarsson and questions about the STD chip to C. Barlag.